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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/419,386	10/15/1999	BRIAN FOX	TRI-003	1198

7590 10/11/2002

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EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/419,386	Applicant(s) FOX ET AL.	
	Examiner Reginald G. Bragdon	Art Unit 2186	

-- The MAILING DATE of this communication app ars on the cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-32* is/are pending in the application.

4a) Of the above claim(s) *4-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14-19 and 21-32* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 23 August 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/419,386 is acceptable and a CPA has been established. An action on the CPA follows.

Information Disclosure Statement

2. The information disclosure statement filed 23 August 2002 has been considered by the Examiner. See the attached PTO-1449.

U.S. Patents 4,870,302 (Freeman), 5,489,858 (Pierce et al.), and 5,600,271 (Erickson et al.) have been crossed off the PTO-1449 since these documents were previously considered in the IDS submitted 02 January 2002.

Claim Objections

3. Claim 16-18 are objected to because of the following informalities: in claim 16, line 2, "in to" should be --into--.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Gilson (5,361,373).

As per claim 1, Gilson teaches a Field Programmable Gate Array (FPGA) 12 including a computing device 10 ("configurable system on a chip"). The computing device 10 includes a configuration memory array 20 ("configurable system logic"). A "system bus" is represented by the bus interconnecting the host I/F, configuration memory array, and reconfigurable instruction execution unit. Configuration data is loaded into the configuration memory array 20 over the bus by Host 40 ("configuring a memory cell in the CSL using the system bus"). See column 5, lines 46-50. The configuration data is then utilized to configure the reconfigurable instruction execution unit ("reading the memory cell in the CSL using the system bus"). See column 7, lines 26-35.

6. Claims 1, 14-19, and 21-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Gittinger et al. (5,668,815).

As per claim 1, Gittinger et al. teaches a microcontroller formed on a single monolithic semiconductor substrate ("configurable system on a chip"). The microcontroller includes a processor core 16 ("CPU"), DMA control 20, a central bus 34 ("system bus") and internal memory 30 ("configurable system logic"). See figure 1. The internal memory 30 is initialized ("configuring a memory cell in the CSL using the system bus") with a selected background

pattern. See column 12, lines 40-42. Then the background pattern is read from the memory ("reading the memory cell in the CSL using the system bus"). See column 13, lines 21-23.

As per claim 21, Gittinger et al. teaches a microcontroller formed on a single monolithic semiconductor substrate ("configurable system on a chip"). The microcontroller includes a processor core 16 ("CPU"), DMA control 20, a central bus 34 ("system bus") and internal memory 30 ("configurable system logic"). See figure 1. The processor core 16 controls the operation of initiating the configuration as set forth at column 13, line 64, to column 14, line 3 ("initiating configuration..."). The DMA controller then takes over operation. See column 14, lines 4-19 ("passing control..."). The internal memory 30 is initialized ("configuring a memory cell in the CSL using the system bus") with a selected background pattern. See column 12, lines 40-42.

As per claim 14, Gittinger et al. teaches that the internal memory 30 is part of the addressable memory space of the system (and therefore the system bus). See column 12, lines 14-18.

As per claims 15 and 18, Gittinger et al. teaches that the DMA controller reads the pattern out of the internal memory. See column 13, lines 21-23.

As per claims 16-17, Gittinger et al. teaches that the internal memory is a random access memory at column 6, lines 61-65.

As per claim 19, Gittinger et al. teaches that the central bus 34 is used for interconnecting the elements of the microcontroller as well as configuring the memory 30.

As per claim 22, Gittinger et al. teaches that the DMA controller configures the internal memory.

As per claim 23, Gittinger et al. teaches that the DMA controller reads the pattern out of the internal memory. See column 13, lines 21-23.

As per claim 24, Gittinger et al. teaches that the internal memory 30 is part of the addressable memory space of the system (and therefore the system bus). See column 12, lines 14-18.

As per claims 25-26, Gittinger et al. teaches that the internal memory is a random access memory at column 6, lines 61-65.

As per claim 27, Gittinger et al. teaches that the DMA controller reads the pattern out of the internal memory. See column 13, lines 21-23.

As per claim 28, Gittinger et al. teaches that the central bus 34 is used for interconnecting the elements of the microcontroller as well as configuring the memory 30.

As per claim 29, Gittinger et al. teaches use of an interrupt signal to indicate that configuration is occurring in the system. See column 14, lines 18-19. Gittinger et al. teaches further signals (such a PIO pin) which indicate that the microcontroller is operating in a test mode of operation.

As per claim 30 Gittinger et al. teaches a microcontroller formed on a single monolithic semiconductor substrate ("configurable system on a chip"). The microcontroller includes a processor core 16 ("CPU"), DMA control 20, a central bus 34 ("system bus") and internal memory 30 ("configurable system logic"). See figure 1. The processor core 16 controls the operation of initiating the configuration as set forth at column 13, line 64, to column 14, line 3 ("initiating configuration..."). The DMA controller then takes over operation. See column 14, lines 4-19. The internal memory 30 is initialized with a selected background pattern using the

DMA controller ("configuring a memory cell"). See column 12, lines 40-42. Gittinger et al. teaches that the DMA controller reads the pattern out of the internal memory ("reading a memory cell"). See column 13, lines 21-23. Gittinger et al. further teaches use of an interrupt signal to indicate that configuration is occurring in the system. See column 14, lines 18-19. Gittinger et al. teaches further signals (such a PIO pin) which indicate that the microcontroller is operating in a test mode of operation ("selecting a signal").

As per claim 31, Gittinger et al. teaches that the DMA controller is the first and second device.

As per claim 32, Gittinger et al. teaches that the bus 34 is controlled by the DMA controller or the processor core depending upon which device is accessing the internal memory.

Allowable Subject Matter

7. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 23 August 2002 have been fully considered but they are not persuasive.

With respect to Applicant's arguments concerning the "selectable one..." language of claim 1, these are not persuasive. The claim does not set forth "what" does the act of selecting. A system designer selecting one particular element to perform the "controlling the system bus for

configuration" would meet the claim limitation. For example, based on the claim language, a designer may have selected a CPU to perform the controlling of the system bus for configuration, and a DMA device or external control device would not need to be present in the system in order to meet the claim limitations.

Therefore, in Gilson, a system designer selected the host 40 (a "CPU") as the device to configure the FPGA. It is not necessary for Gilson to teach a DMA controller which controls the system bus for configuration in order to anticipate claim 1.

With respect to Gittinger et al., Applicant argues that memory 30 is not a configurable system logic. However, the broad limitation of "configurable system logic" is taught by the internal memory 30 since the memory 30 is configurable (by virtue of being able to store data) and contains logic within the microcontroller system.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taylor (6,347,346) and Hanrahan et al. (6,349,346) teach a reconfigurable system including a DMA device and a system bus.

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
October 1, 2002